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40GBASE–SR4 QSFP+ Optical Engine

Preliminary

TYPE NAME: Q45G-WG515-110(ENG)

Product Description:

LuxNet Q45G-WG515-110(ENG) 40GBASE-SR4 QSFP+ Optical Engine is designed for high-speed and high-performance Data Communication applications and Fiber Channel Networking/Storage applications. This device is integrated with an 850nm VCSEL array, an 850nm Photo Detector array, Quad VCSEL driver, Quad transimpedance amplifier, plastic lens array and high speed flex board. The product is especially designed for 40Gbps transceiver module, 40Gbps Active Optical Cable module and systems usage.

Product Specifications:

Application:	40GBASE–SR4 QSFP+ Transceiver and Active Optical Cable
Optical connector:	12 fiber MT connector
Tx nominal bit rate:	10.3Gbps x 4 channel
Rx nominal bit rate:	10.3Gbps x 4 channel
Required operating length:	0.5 ~ 100M for 50/125um OM3 / 150M for 50/125um OM4
TIA:	Gigoptix HXR5004A
LD Driver:	Gigoptix HXT5004A

Absolute Maximum Ratings

Parameter	Symbol	Units	Min	Max	Note
Operating Temperature (case)	Top	^{o}C	0	70	
Storage Temperature	Tstg	^{o}C	-40	+85	
Solder Reflow Temperature (10 sec)	STEM	^{o}C	-	260	

Electro Characteristics (T = 25°C, unless noted otherwise):

Parameter	Symbol	Units	Min	Typical	Max	Test condition
Supply Voltage	V_{cc}	Volts		3.30		
Transmitter Supply Current	$I_{cc}T$	mA		82		V_{cc}=3.3V
Receiver Supply Current	IccR	mA		141		V_{cc}=3.3V

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Optical Characteristics (T = 25°C, unless noted otherwise):

Transmitter						
Parameter	Symbol	Units	Min	Typical	Max	Test condition
Center Wavelength	λ	nm	840	850	860	
RMS spectral width	Δλ	nm			0.65	
Average launch power, each lane	Pf	dBm	-7.6		2.4	Iop=6mA
Optical Modulation Amplitude (OMA), each lane		dBm	-5.6		3	
Difference in launch power between any two lanes (OMA)		dB			4	
Extinction ratio	ER	dB	3			Iop=6mA
Receiver reflectance	ORL	dB			-12	
Average launch power of OFF transmitter, each lane		dBm			-30	
Receiver						
Parameter	Symbol	Units	Min	Typical	Max	Test condition
Damage threshold		dBm	3.4			
Average power at receiver input, each lane		dBm	-9.5		2.4	12Gbps, PRBS31, BER=10^{-12}, ER=4.5dB, Output Differential Voltage = Min.290mV
Receiver reflectance	ORL	dB			-12	
Optical Modulation Amplitude (OMA), each lane		dBm			3	
Peak Power, each lane		dBm			4	

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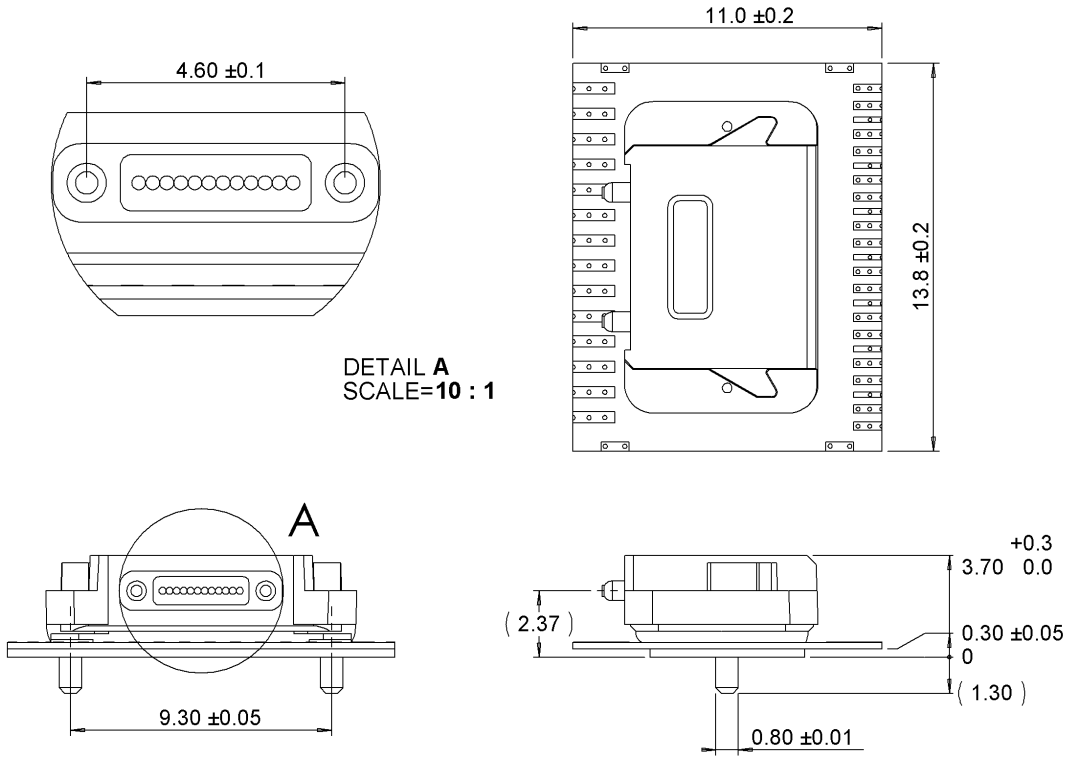
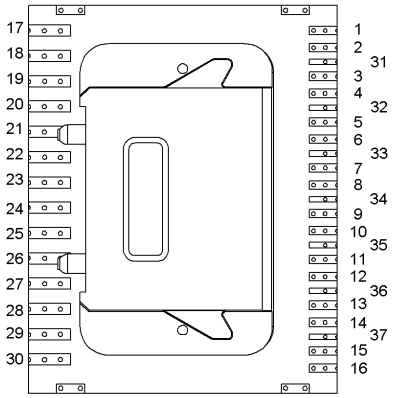
Outline Dimension(mm):

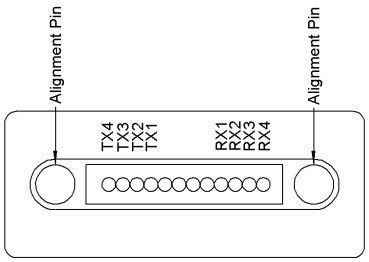


Electrical IO Assignment:



Top View

Optical IO Assignment:



Front View

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PIN NUMBER	PIN NAME	Description
1	DIN4N	Differential high-speed **Data Input** pin P is the positive (non-inverted) node and N is the negative (inverted) node. The differential inputs are internally terminated with 100Ω. Pin P is the positive (non-inverted) node and pin N is the negative (inverted) node.
2	DIN4P	
3	DIN3N	
4	DIN3P	
5	DIN2N	
6	DIN2P	
7	DIN1N	
8	DIN1P	
9	DOUT1P	Differential high-speed **Data Output** pads, P is the positive (non-inverted) node and N is the negative (inverted) node.
10	DOUT1N	
11	DOUT2P	
12	DOUT2N	
13	DOUT3P	
14	DOUT3N	
15	DOUT4P	
16	DOUT4N	
17	NOTINTT	The active-low **Interrupt** (NOTINT) signal notifies the external microcontroller about driver events. These events include VCSEL operating voltage violations (VVL_x, VVH_x), input loss of signal, input signal detect and control loop faults. The polarity of the interrupt can be inverted by programming. The state of the pin may be read through the management interface.
18	SDAT	The **Serial Data** pin (SDA) is a bidirectional pin for the data signal. The pin can be tied directly to VDD of 3.3V or 2.5V. The SDA pin is I^2C-bus compatible. This pad is a CMOS input/output pad. The pullup is 10 kΩ.
19	SCLT	The **Serial Clock** pin (SCL) is the clock signal of the serial interface. The pin can be tied to VDD 3.3V or 2.5V. The SCL input is I^2C-bus compatible and can be clocked at up to 1000kHz. The pullup is 10kΩ.

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20	IMON	The **Monitor Current** output (IMON) is an analog output with two functions. The IMON Select Register controls a multiplexer to select either a scaled replica of the unit current, a temperature proportional current, or, a scaled copy of the average current of a specific channel. By measuring the unit current during production, process dependencies are isolated and an estimate of the settings can be calculated. The average current and modulation current are derived from the unit current (I_U). The copy of the average current of an individual channel is used for real time diagnostic functions. The output is connected to ground via a resistor. A microcontroller with an integrated analog to digital converter can monitor this output and service queries from the host system.
21	LDIS	The **Laser Disable** pin (LDIS) is a global output disable signal that will set Iavg and Imod to 0 when it is high, regardless of other settings. The pin can be left unconnected and the device will operate normally. The state of the pin may be read through the management interface.
22	VCCT	Positive supply of driver stages and VCSEL anodes
23	GNDT	Negative supply, substrate
24	VCC2	Positive supply of Limiting amplifier stage
25	GNDR	Negative supply, substrate
26	VCC1	Positive supply of TIA stage
27	RSSI	The **Receiver Signal Strength Indicator** output (RSSI) pad is an analog output that sources a current proportional to the average photo- detector current on the selected channels. The output is used during manufacturing for active alignment. As well, the output can be configured to produce a temperature proportional output.
28	NOTINTR	The active- low **Interrupt** (NOTINT) signals notifies the microcontroller about signal detect events such as signal detect and loss of signal when the events are unmasked. In systems using polling- based firmware, this input may be left unconnected.

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29	SCLR	The **Serial Clock** pad (SCL) is the clock input signal of the serial interface. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SCL input is I^2C- bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.
30	SDAR	The **Serial Data** pad (SDA) is a bidirectional pad for the serial data signal. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SDA pad is I^2C- bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.
31	GNDT	Negative supply, substrate
32		
33		
34		
35	GNDR	Negative supply, substrate
36		
37		

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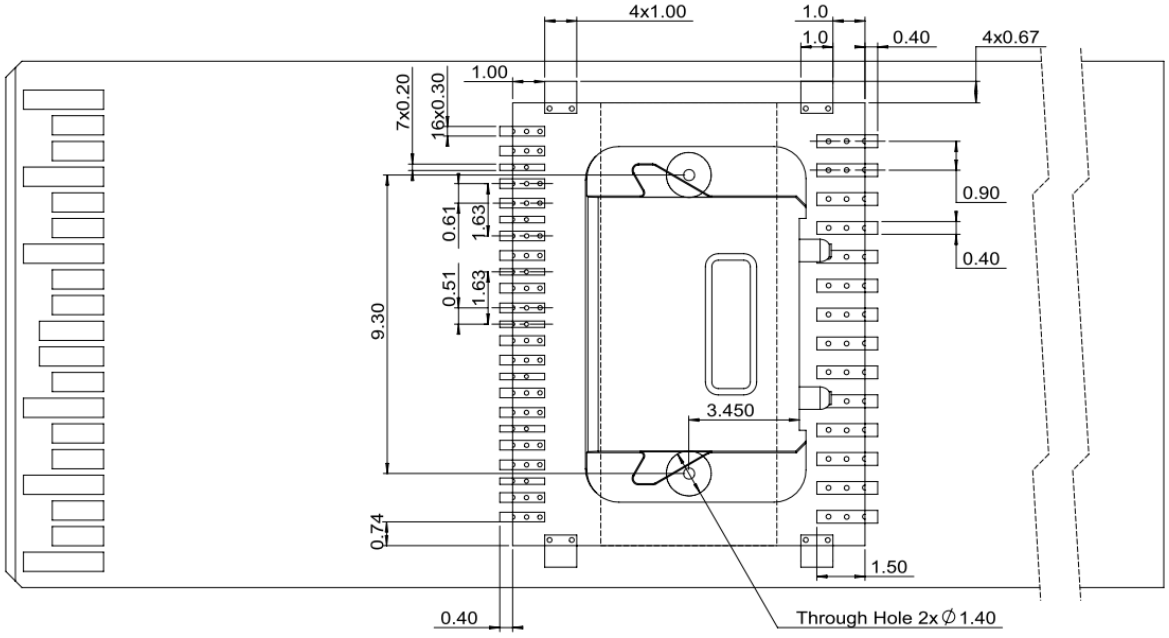
Application Note

1. Landing Pattern



2. Flex-Board outline