LUXNET CORPORATION

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40G PSM4 Array ROSA (Preliminary)

Q15S-XD95x-xxx Series

TYPE NAME: Q15S-XD95x-xxx (BR-GM99-xx)

Product Description:

LuxNet Q15S-XD95x-xxx 40GBASE PSM4 array ROSA is designed for high-speed and high-performance Data Communication applications and Fiber Channel Networking/Storage applications. This device is integrated with 1310/1550nm Photo Detector array, Quad transimpedance amplifier, plastic lens array and high speed flex board. The product is especially designed for 40Gbps QSFP+ transceiver module.

Product Specifications:

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min.	Max.	Note
Operating Temperature	T_{op}	°C	-5	85	Case Temperature
Storage Temperature	T_{stg}	°C	-40	85	
Solder Reflow Temperature	T_s	°C	-	260	Max 10 seconds max.
Power Supply Voltage	V_P	V	-0.3	4.5	
Optical Power	P_{in}	dBm	-	5	

Electro-Optical Characteristics (T = 25°C, unless noted otherwise):

Parameter	Symbol	Unit	Min.	Typ	Max.	Test Condition
Supply Voltage	Vcc	V	3.0	3.3	3.6	Tc=0°C~85°C
Supply Current	Icc	mA	-	-	230	Vcc= 3.3V@ Tc=0°C~85°C
Sensitivity	S	dBm	-	-	-14.6	λ=1310nm , Speed=10.3125Gbps PRBS=2^31-1, BER=10^-12, ER=4.5dB Tc=0°C~85°C
Wavelength	λ	nm		1310		Tc=0°C~85°C
Dark Current	Id	nA	-	20	50	Vr= -5V
Optical Return Loss	ORL	dB	-	-	-12	SMF MT/PC
Overload Power	Pload	dBm	+1.5	-	-	PRBS=2^31-1, BER=10^-12, ER=4.5dB Tc= 0°C~85°C
Rise /Fall Time	τ_r / τ_f	ps	-	-	30	V_R=2V,20-80%,RL=50Ω
Cut-off Frequency	fc	GHz	9			V_R=2V,RL=50Ω

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Parameter	Symbol	Unit	Min.	Typ	Max.	Test Condition
Eye mask margin	EMM	%	10	-	-	Mask according to IEEE802.3ba Annex 86A Table 86A3; Tc=0˚C~85˚C Pin= 1.5 ~ -12.6dBm
Stress receiver sensitivity in OMA	Ssen	dBm	-	-	-10.3	λ=1310nm , Speed=10.3125Gbps PRBS=2^31-1, BER=10^-12, Tc=0°C~85°C

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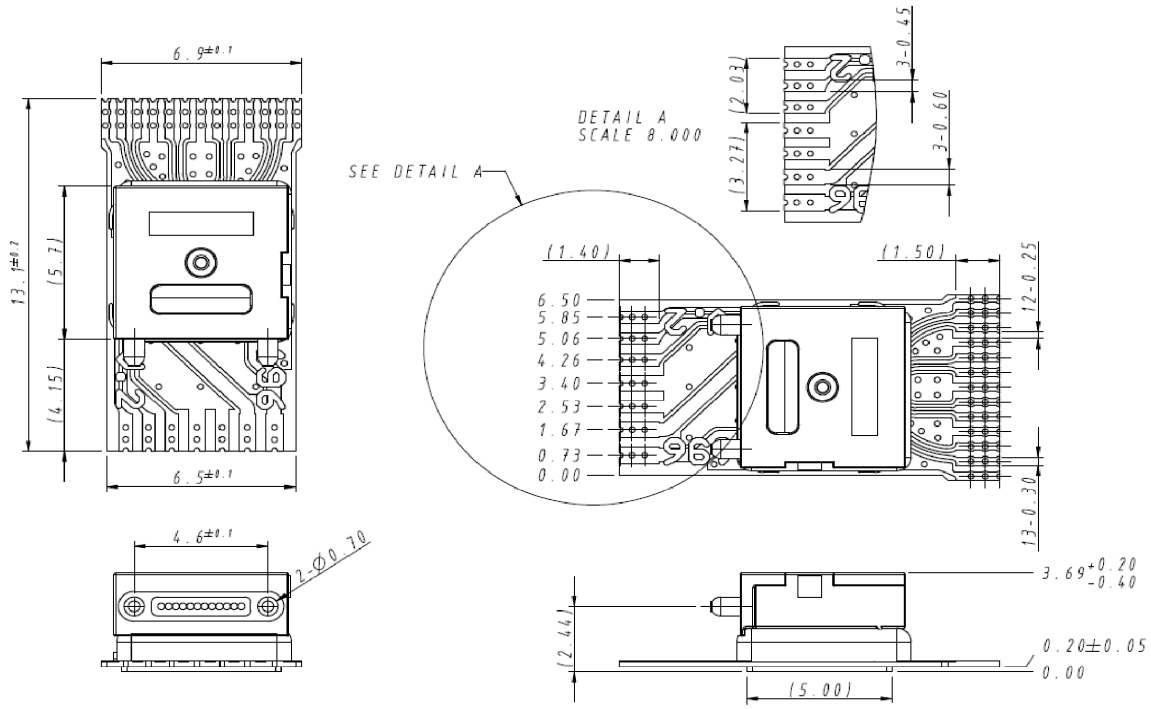
Outline Dimension(mm):



Electrical IO Assignment:

Optical IO Assignment:

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PIN NUMBER	PIN NAME	Description
1	Z01N	Differential high-speed **Data Output** pads, P is the positive (non-inverted) node and N is the negative (inverted) node.
2	Z01P	
3	Z02N	
4	Z02P	
5	Z03N	
6	Z03P	
7	Z04N	
8	Z04P	
9	VCC	Positive supply of TIA stage
10		
11	GND	Negative supply, substrate
12		
13	LOS	●Global hardware LOS status output (100kΩ pull-up). ●Pin Type: Digital Output. ●Status: Open-drain with 100kΩ pull-up.
14	SCL	●I^2C clock interface. Pull-up resistor is required off-chip. ●Pin Type: Digital Input. ●Status: None ●The I^2C serial interfaces supports a single-master fast-mode (400kb/s) signalling. ●The I^2C slave with a default addresses of B8h. ●The host-supplied SCL input to TIA is used to positive edge clock data into TIA and negative clock data out of TIA. ●SCL pins are normally pulled HIGH with external 10kΩ resistors.
15	SDA	●I^2C data interface. Pull-up resistor is required off-chip. ●Pin Type: Digital I/O. ●Status: Open-drain. ●The I^2C serial interfaces supports a single-master fast-mode (400kb/s) signalling. ●The I^2C slave with a default addresses of B8h. ●The SDA pin is bi-directional for serial data transfer. This pin is open-drain and may be wire-OR'ed with any other open-drain devices on the same bus. ●SDA pins are normally pulled HIGH with external 10kΩ resistors.

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16	GND	Negative supply, substrate
17		
18		
19		
20		